Yousef Maitah

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Education

University of Michigan Ann Arbor, MI

Bachelor of Science in Electrical Engineering *Aug. 2021 – Dec 2025*

- GPA: 3.7/4.0
- Relevant Coursework: Computer Organization, Digital Circuits, Logic Design, Semiconductor Devices, Quantum Nanotechnology, Control Systems Analysis and Design, Programming and Data Structures, Signals and Systems
- Awards/Honors: James B. Angell Scholar, Dean's List, University Honors

Experience

Electrical Engineering Intern May 2024 – Aug. 2024

Nexteer Automotive *Saginaw, MI*

∗ Developed an ignition test box for a Steer-by-wire project, improving reliability through enhanced test coverage
∗ Analyzed OEM design, safety, and software requirements to strengthen feature function mapping
∗ Authored detailed work instructions, increasing test efficiency and knowledge transfer
∗ Collaborated cross-functionally to drive effective teamwork and problem-solving

Electrical Engineering Intern May 2023 – Aug. 2023

Nexteer Automotive *Auburn Hills, MI*

∗ Designed and executed test procedures for ECU-based electric power steering, improving system reliability
∗ Configured and debugged harness/test bench setups, reducing setup time and improving testing efficiency by 30%
∗ Analyzed test data to identify patterns and anomalies, providing detailed reports and recommendations
∗ Troubleshot hardware/software integration issues, ensuring compliance with customer specifications

Projects

8-bit Dual-Mode Ripple-Carry Adder | *Cadence Virtuoso* Nov 2023 – Dec. 2024

∗ Designed and implemented an 8-bit ripple-carry adder optimized for both addition and accumulation tasks
∗ Utilized Differential Cascode Voltage Switch Logic (DCVSL) to improve speed and reduce power consumption
∗ Optimized transistor sizing to balance performance and efficiency, achieving a 1 GHz clock frequency in high-speed mode while reducing power consumption by 17.2% in low-power mode compared to traditional mirror adders

Four-Function Calculator | *Verilog* April 2024

∗ Developed a four-function calculator on an FPGA using Verilog, implementing RTL design principles
∗ Designed control logic for 11-bit 2's complement arithmetic, integrating user inputs via buttons and switches
∗ Implemented overflow detection with indicator LEDs and managed timing constraints using a 50MHz clock

CPU Cache Simulator | *C* December 2024

∗ Developed a cache simulator using caching, clock, and LRU heuristics to simulate various cache configurations
∗ Implemented algorithms to link file types, manage memory addresses in page tables, and optimize evictions

Skills

Languages: C/C++, Python, SystemVerilog, MATLAB, HTML/CSS
Tools: Arduino, Cadence Virtuoso, Git, Linux, ModelSim, Oscilloscope, Quartus, Simulink, Vector Tools, VS Code
Techniques: Circuit Design, Communication Protocols, FPGA, Hardware Validation, Soldering

Extracurriculars

EPS Driven May 2024 – Aug 2024

- Designed and built an electric go-kart, integrating power and control systems under budget constraints
- Applied embedded systems knowledge for motor control and sensor integration