Yousef Maitah

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Education

University of Michigan — Ann Arbor, MI

Bachelor of Science in Electrical Engineering, GPA: 3.7/4.0 — *Aug. 2021 – Dec 2025*

- **Coursework:** Logic Design, Digital Circuits, Computer Architecture, Control Systems, Signals and Systems, Programming and Data Structures, Semiconductor Devices, Electromagnetics
- **Awards/Honors:** James B. Angell Scholar, Dean's List, University Honors

Experience

General Motors — Milford, MI

Engineering Intern - Driveline Development and Integration — *May 2025 – Aug. 2025*

- Supported driveline mechatronics and controls integration efforts on the D2-2 AWD system (Chevy Equinox / GMC Terrain) by collaborating with calibration engineers to investigate and resolve system performance issues
- Conducted on-road and off-road data collection for wheel torque and driveline dynamics using instrumentation, including specialized evaluations in cold box environments (-40°C) and sand dunes terrain testing
- Collaborated cross-functionally with technical specialists, DREs, suppliers to assess halfshaft NVH characteristics
- Documented work instructions and post-test analysis reports to inform engineering decisions

Nexteer Automotive — Saginaw, MI

Engineering Intern - Systems Application Team — *May 2024 – Aug. 2024*

- Developed an ignition test box for a Steer-by-wire project, improving reliability through enhanced test coverage
- Analyzed OEM design, safety, and software requirements to strengthen feature function mapping
- Authored detailed work instructions, increasing test efficiency and knowledge transfer
- Collaborated cross-functionally to drive effective teamwork and problem-solving

Nexteer Automotive — Auburn Hills, MI

Engineering Intern - ECU HiL Team — *May 2023 - Aug. 2023*

- Designed and executed test procedures for ECU-based electric power steering, improving system reliability
- Configured and debugged harness/test bench setups, reducing setup time and improving testing efficiency by 30%
- Analyzed test data to identify patterns and anomalies, providing detailed reports and recommendations

Projects

Out-of-Order RISC-V Processor | *SystemVerilog* — Oct. 2025 – Dec. 2025

- Designed a fully synthesizable N-way superscalar out-of-order processor with advanced features such as instruction prefetching and early branch resolution
- Implemented a MIPS R10000-style microarchitecture with register renaming

Smart Room Occupancy Monitoring System | *C* — Oct. 2025 – Dec. 2025

- Designed and built an IoT room-occupancy sensing system using an ESP32 microcontroller to detect and count people entering/exiting a space in real time
- Integrated Time-of-Flight and PIR sensors to improve detection accuracy and direction tracking
- Implemented wireless data transmission to a central server for live occupancy monitoring

8-bit Dual-Mode Ripple-Carry Adder | *Cadence Virtuoso* — Nov 2024 – Dec. 2024

- Designed and implemented an 8-bit ripple-carry adder optimized for both addition and accumulation tasks
- Optimized transistor sizing to balance performance and efficiency, achieving a 1 GHz clock frequency in high-speed mode while reducing power consumption by 17.2% in low-power mode compared to traditional mirror adders

Skills

Languages: C/C++, Python, SystemVerilog, MATLAB, HTML/CSS
Tools: Altium Designer, Arduino, Cadence Virtuoso, Git, Linux, Oscilloscope, Simulink, Vector Tools, VS Code
Techniques: Circuit Design, Communication Protocols, FPGA, Hardware Validation, Soldering, System Design