

# Yousef Maitah

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## EDUCATION

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### University of Michigan

*Bachelor of Science in Electrical Engineering*

Ann Arbor, MI

Aug. 2021 – Dec 2025

- GPA: 3.7/4.0
- Relevant Coursework: Signals and Systems, Control Systems Analysis and Design, Programming and Data Structures, Computer Organization, Digital Circuits, Logic Design, Semiconductor Devices, Electromagnetics
- Awards/Honors: James B. Angell Scholar, Dean's List, University Honors

## EXPERIENCE

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### Engineering Intern

May 2025 – Aug. 2025

*General Motors - Driveline Development and Integration*

*Milford, MI*

- \* Expected to contribute to system development, validation, and testing of driveline components
- \* Collaborate with cross-functional teams to evaluate driveline performance under varying load conditions
- \* Apply knowledge of hardware validation, system-level design, and embedded control for automotive systems

### Engineering Intern

May 2024 – Aug. 2024

*Nexteer Automotive - Systems Application Team*

*Saginaw, MI*

- \* Developed an ignition test box for a Steer-by-wire project, improving reliability through enhanced test coverage
- \* Analyzed OEM design, safety, and software requirements to strengthen feature function mapping
- \* Authored detailed work instructions, increasing test efficiency and knowledge transfer
- \* Collaborated cross-functionally to drive effective teamwork and problem-solving

### Engineering Intern

May 2023 – Aug. 2023

*Nexteer Automotive - ECU HIL Team*

*Auburn Hills, MI*

- \* Designed and executed test procedures for ECU-based electric power steering, improving system reliability
- \* Configured and debugged harness/test bench setups, reducing setup time and improving testing efficiency by 30%
- \* Analyzed test data to identify patterns and anomalies, providing detailed reports and recommendations
- \* Troubleshoot hardware/software integration issues, ensuring compliance with customer specifications

## PROJECTS

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### Four-Function Calculator | Verilog

April 2024

- \* Developed a four-function calculator on an FPGA using Verilog, implementing RTL design principles
- \* Designed control logic for 11-bit 2's complement arithmetic, integrating user inputs via buttons and switches
- \* Implemented overflow detection with indicator LEDs and managed timing constraints using a 50MHz clock

### CPU Cache Simulator | C

December 2024

- \* Developed a cache simulator using caching, clock, and LRU heuristics to simulate various cache configurations
- \* Implemented algorithms to link file types, manage memory addresses in page tables, and optimize evictions

## SKILLS

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**Languages:** C/C++, Python, SystemVerilog, MATLAB, HTML/CSS

**Tools:** Arduino, Cadence Virtuoso, Git, Linux, ModelSim, Oscilloscope, Quartus, Simulink, Vector Tools, VS Code

**Techniques:** Circuit Design, Communication Protocols, FPGA, Hardware Validation, Soldering

## EXTRACURRICULARS

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### EPS Driven

May 2024 – Aug 2024

- Designed and built an electric go-kart, integrating power and control systems under budget constraints
- Applied embedded systems knowledge for motor control and sensor integration